WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, which comprises the steps of:

forming a device isolation film defining a device region in a silicon substrate;

depositing a gate electrode material film on the substrate and patterning the deposited gate electrode material film so as to form a gate electrode on the substrate;

implanting impurity ions into the substrate so as to form junction regions in the substrate;

forming an interlayer insulating film on the substrate and selectively patterning the interlayer insulating film so as to partially expose the surface of the substrate; and

forming a two-layered contact plug consisting of a first contact layer having high impurity concentration and a second contact layer having low impurity concentration, on the interlayer insulating film including the exposed surface of the substrate.

2. The method of Claim 1, wherein further comprises the step of treating the exposed surface of the silicon substrate by a process selected from the group consisting of

a dry cleaning process, a wet cleaning process, a native oxide removal process, a thermal treatment process using hydrogen gas, and a surface treatment process using a laser.

3. The method of Claim 2, wherein the dry cleaning process is carried out by treating the substrate surface with a plasma mixture of NF_3, O_2, He and N_2 of a suitable mixing ratio at a plasma power of less than 2 kW for a period shorter than 5 minutes, the wet cleaning process is carried out by treating the substrate surface with a diluted solution of H_2O_2, H_2SO_4, NF_4OH, HF, BOE or a combination thereof, the native oxide removal process is carried out by thermally treating the substrate surface with a plasma mixture of NF_3 and N_2 gases of a suitable mixing ratio at a temperature of 100-500 °C for a period shorter than 10 minutes, and the process of thermally treating the substrate surface with hydrogen gas is carried out by an *in situ* process or an *ex situ* process using 1-10 slm hydrogen at a thermal treatment temperature of 700-1,000 °C under a pressure of 1 mtorr-100 torr for a period shorter than 30 minutes.

4. The method of Claim 2, wherein the dry cleaning process, the wet cleaning process, the native oxide removal

process, the thermal treatment process using hydrogen gas, and the surface treatment process using a laser are used independently or in combination.

5. The method of Claim 2, which further comprises the step of implanting an impurity into the exposed surface of the silicon substrate, after the step of treating the exposed surface of the silicon substrate.

6. The method of Claim 5, wherein the impurity is P or As, which is implanted at an implantation energy of 10-100 KeV and a dose of 1E10-1E20 atoms/cm^3.

7. The method of Claim 1, wherein the first contact plug layer is formed of polycrystalline silicon or monocrystalline silicon.

8. The method of Claim 1, wherein the first or second contact plug layer is deposited by atmospheric pressure chemical vapor deposition or low-pressure chemical vapor deposition using DCS/H_2/PH_3, MS/H_2/PH_3 or MS/PH_3 gas.

9. The method of Claim 9, wherein the MS gas is used at a flow rate of 100-500 sccm, the DCS gas is used at the

flow rate of 100-500 sccm, and the H_2 gas is used at a flow rate of 500-20,000 sccm.

10. The method of Claim 8, wherein the deposition of the first or second contact plug layer is carried out under a pressure of 1-200 torr at a temperature of 500-700 °C.

11. The method of Claim 1, wherein the first contact plug layer is formed to a thickness of 50-500 Å while using 1% PH_3 at a flow rate of 100-1,000 sccm, and P impurities at a concentration of 1E20 to 5E20 atoms/cm^3.

12. The method of Claim 1, wherein the second contact plug layer is formed to a thickness of 500-5,000 Å while using 1% PH_3 at a flow rate of 100-1,000 sccm, and P impurities at the concentration of 1E19 to 2E20 atoms/cm^3.

13. A method for fabricating a semiconductor device, which comprises the steps of:

forming a device isolation film defining a device region in a silicon substrate;

depositing a conductive layer on the substrate and patterning the deposited conductive layer so as to form a gate electrode on the substrate;

implanting impurity ions into the substrate so as to form junction regions in the substrate;

forming an interlayer insulating film on the substrate and selectively patterning the interlayer insulating film so as to partially expose the surface of the substrate;

treating the exposed surface of the substrate; and

forming a two-layered contact plug consisting of a first contact plug layer having high impurity concentration and a second contact plug layer having low impurity concentration, on the interlayer insulating film including the exposed surface of the substrate.

14. The method of Claim 13, wherein the step of treating the exposed surface of the silicon substrate is carried out by a process selected from the group consisting of a dry cleaning process, a wet cleaning process, a native oxide removal process, a thermal treatment process using hydrogen gas, and a surface treatment process using a laser.

15. The method of Claim 14, wherein the dry cleaning process is carried out by treating the substrate surface with a plasma mixture of NF_3, O_2, He and N_2 of a suitable mixing ratio at a plasma power of less than 2 kW for a period shorter than 5 minutes, the wet cleaning process is

carried out by treating the substrate surface with a diluted solution of H_2O_2, H_2SO_4, NF_4OH, HF, BOE or a combination thereof, the native oxide removal process is carried out by thermally treating the substrate surface with a plasma mixture of NF_3 and N_2 gases of a suitable mixing ratio at a temperature of 100-500 °C for a period shorter than 10 minutes, and the process of thermally treating the substrate surface with hydrogen gas is carried out by an *in situ* process or an *ex situ* process using 1-10 slm hydrogen at a thermal treatment temperature of 700-1,000 °C under a pressure of 1 mtorr-100 torr for a period shorter than 30 minutes.

16. The method of Claim 13, which further comprises the step of implanting an impurity into the exposed surface of the silicon substrate, after the step of treating the exposed surface of the silicon substrate, in which the impurity is P or As, which is implanted at an implantation energy of 10-100 KeV and a dose of 1E10-1E20 atoms/cm^3.

17. The method of Claim 13, wherein the first or second contact plug layer is deposited by atmospheric pressure chemical vapor deposition or low-pressure chemical vapor deposition using $DCS/H_2/PH_3$, $MS/H_2/PH_3$ or MS/PH_3 gas.

18. The method of Claim 17, wherein the MS gas is used at a flow rate of 100-500 sccm, the DCS gas is used at the flow rate of 100-500 sccm, and the H_2 gas is used at a flow rate of 500-20,000 sccm.

19. The method of Claim 13, wherein the first contact plug layer is formed to a thickness of 50-500 Å while using 1% PH_3 at a flow rate of 100-1,000 sccm, and P impurities at a concentration of 1E20 to 5E20 atoms/cm^3, and the second contact plug layer is formed to a thickness of 500-5,000 Å while using 1% PH_3 at a flow rate of 100-1,000 sccm, and P impurities at the concentration of 1E19 to 2E20 atoms/cm^3.